



NOV 09 2007

Attorney Docket No.: CYPR-  
CD01213M

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
Patent Application

Inventor(s): Nemecek et al.

Group Art Unit: 2123

Filed: November 1, 2001

Examiner: Proctor, J.

Application No.: 10/001,478

Title: IN-CIRCUIT EMULATOR AND POD SYNCHRONIZED BOOT

**Form 1449**

**U.S. Patent Documents**

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
A	2002/0052729	05-02-2002	Kyung et al.				
B	2002/0116168	08-22-2002	Kim				
C	2002/0156885	10-24-2002	Thakkar				
D	2002/0156998	10-24-2002	Casselman				
E	2003/0056071	03-20-2003	Triewe et al.				
F	2003/0149961	08-07-2003	Kawai et al.				
G	4,176,258	11-27-1979	Jackson				
H	5,127,103	06-30-1992	Hill et al.				
I	5,202,687	04-13-1993	Distinti				
J	5,321,828	06-14-1994	Phillips et al.				
K	5,325,512	06-28-1994	Takahashi				
L	5,331,571	07-19-1994	Aronoff et al.				
M	5,357,626	10-18-1994	Johnson et al.				
N	5,493,723	02-20-1996	Beck et al.				
O	5,546,562	08-13-1996	Patel				
P	5,559,996	09-24-1996	Fujioka et al.				
Q	5,572,665	11-05-1996	Nakabayashi				
R	5,574,892	11-12-1996	Christensen				
S	5,587,957	12-24-1996	Kowalczyk et al.				
T	5,590,354	12-31-1996	Klapproth et al.				
U	5,630,052	05-13-1997	Shah				
V	5,630,102	05-13-1997	Johnson et al.				
W	5,663,900	09-02-1997	Bhandari et al.				
X	5,691,898	11-25-1997	Rosenberg et al.				
Y	5,752,013	05-12-1998	Christensen et al.				
Z	5,802,290	09-01-1998	Casselman				
A1	5,805,792	09-08-1998	Swoboda et al.				
B1	5,889,988	03-30-1999	Held				
C1	5,911,059	06-08-1999	Profit, Jr.				
D1	5,964,893	10-12-1999	Circello et al.				
E1	5,999,725	12-07-1999	Barbier et al.				
F1	6,009,270	12-28-1999	Mann				
G1	6,016,554	01-18-2000	Skrovan et al.				
H1	6,016,563	01-18-2000	Fleisher				
I1	6,034,538	03-07-2000	Abramovici				
J1	6,058,263	05-02-2000	Voith				
K1	6,075,941	06-13-2000	Itoh et al.				
L1	6,094,730	07-25-2000	Lopez et al.				
M1	6,107,826	08-22-2000	Young et al.				
N1	6,144,327	11-07-2000	Distinti et al.				
O1	6,161,199	12-12-2000	Szeto et al.				

	P1	6,173,419	01-09-2001	Barnett				
	Q1	6,185,522	02-06-2001	Bakker				
	R1	6,223,144	04-24-2001	Barnett et al.				
	S1	6,223,272	04-24-2001	Coehlo et al.				
	T1	6,289,300	09-11-2001	Brannick et al.				
	U1	6,298,320	10-02-2001	Buckmaster et al.				
	V1	6,302,268	02-29-2000	Swoboda et al.				
	W1	6,347,395	02-12-2002	Payne et al.				
	X1	6,366,878	04-02-2002	Grunert				
	Y1	6,374,370	04-16-2002	Bockhaus et al.				
	Z1	6,385,742	05-07-2002	Kirsh et al.				
	A2	6,460,172	10-01-2002	Insenser Farre et al.				
	B2	6,466,898	10-15-2002	Chan				
	C2	6,487,700	11-26-2002	Fukushima				
	D2	6,516,428	02-04-2003	Wenzel et al.				
	E2	6,564,179	05-13-2003	Belhaj				
	F2	6,581,191	06-17-2003	Schubert et al.				
	G2	6,618,854	09-09-2003	Mann				
	H2	6,810,442	10-26-2004	Lin et al.				
	I2	6,816,544	11-09-2004	Bailey et al.				
	J2	6,829,727	12-07-2004	Pawloski				
	K2	6,922,821	07-26-2005	Nemecek				
	L2	6,957,180	10-18-2005	Nemecek				
	M2	6,967,960	11-22-2005	Bross et al.				
	N2	7,076,420	07-11-2006	Snyder et al.				
	O2	7,089,175	08-08-2006	Nemecek et al.				
	P2	7,099,818	08-29-2006	Nemecek, Craig				
	Q2	7,162,410	01-09-2007	Nemecek et al.				
	R2	7,236,921	06-26-2007	Nemecek et al.				

#### Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	S2							
	T2							
	U2							

#### Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	V2	Bursky; "FPGA Combines Multiple Interfaces and Logic"; Electronic Design; Vol. 48 No. 20; pages 74-78; October 2, 2000
	W2	Anonymous; "Warp Nine Engineering- the IEEE 1284 Experts- F/Port Product Sheet"; undated web page found at <a href="http://www.fapo.com/fport.htm">http://www.fapo.com/fport.htm</a>
	X2	Anonymous; "F/Port: Fast Parallel Port for the PC: Installation Manual: Release 7.1"; circa 1997; available for download from <a href="http://www.fapo.com/fport.htm">http://www.fapo.com/fport.htm</a>
	Y2	Nam et al.; "Fast Development of Source-Level Debugging System Using Hardware Emulation"; IEEE 2000; pages 40-404
	Z2	Huang et al.; "Iceberg: An Embedded In-Circuit Emulator Synthesizer For Microcontrollers"; ACM 1999; pages 580-585
	A3	Khan et al.; "FPGA Architectures for Asic Hardware Emulators"; IEEE 1993; pages 336-340
	B3	Oh et al.; "Emulator Environment Based on an FPGA Prototyping Board"; IEEE 21-23; June 2000; pages 72-77

	C3	Hong et al.; "An FPGA-Based Hardware Emulator for Fast Fault Emulation"; IEEE 1997; pages 345-348
	D3	Ching et al.; "An In-Circuit-Emulator for TMS320C25"; IEEE 1994; pages 51-56
	E3	Pasternak; "In-Circuit-Emulation in ASIC Architecture Core Designs"; IEEE 1989; pages P6-4.1- P6-4.4
	F3	Melear; "Using Background Modes for Testing, Debugging and Emulation of Microcontrollers"; IEEE 1997; pages 90-97
	G3	Walters; "Computer -Aided Prototyping For ASIC-Based Systems"; 1991; IEEE Design and Test of Computers
	H3	Anonymous; "JEEN JTAG Embedded Ice Ethernet Interface"; August 1999; Embedded Performance, Inc; 3 pages
	I3	Sedory; "A Guide to Debug"; 2004; retrieved on May 20, 2005
	J3	"Microsoft Files Summary Judgment Motions"; February 1999; Microsoft PressPass; retrieved on May 20, 2005 from <a href="http://www.microsfot.com/presspass/press/1999/feb99//Feb99/Calderapr.asp">http://www.microsfot.com/presspass/press/1999/feb99//Feb99/Calderapr.asp</a> ; pages 1-6
	K3	Xerox; "Mesa Debugger Documentation"; April 1979; Xerox Systems Development Department; Version 5.0; pages 1-30
	L3	Stallman et al.; "Debugging with the GNU Source-Level Debugger"; January 1994; retrieved on May 2, 2005 from <a href="http://www.cs.utah.edu">http://www.cs.utah.edu</a>
	M3	Wikipedia.org; "Von Neumann architecture"; retrieved from <a href="http://en.wikipedia.org/wiki/Von_Neumann_architecture">http://en.wikipedia.org/wiki/Von_Neumann_architecture</a> on January 22, 2007; pages 1-5
	N3	Stan Augarten; "The Chip Collection- Introduction- Smithsonian Institute"; "State of the Art"; "The First 256-Bit Static RAM"; retrieved on November 14, 2005 from <a href="http://smithsonianchips.si.edu/augarten/p24.htm">http://smithsonianchips.si.edu/augarten/p24.htm</a>
	O3	"POD- Piece of Data, Plain Old Documentation, Plain Old Dos..."; retrieved on November 14, 2005 from <a href="http://www.auditmypc.com/acronym/POD.asp">http://www.auditmypc.com/acronym/POD.asp</a>
	P3	"Pod-Wikipedia, the free encyclopedia"; retrieved on November 14, 2005 from <a href="http://en.wikipedia.org/wiki/Pod">http://en.wikipedia.org/wiki/Pod</a>
	Q3	"pod-definition by dict.die.net"; retrieved on November 14, 2005 from <a href="http://dict.die.net/pod">http://dict.die.net/pod</a>
	R3	"In-Circuit Emulators- descriptions of the major ICES around"; retrieved on November 14, 2005 from <a href="http://www.algonet.se/~staffann/developer/emulator.htm">http://www.algonet.se/~staffann/developer/emulator.htm</a>
	S3	CYPR-CD00183; "Capturing Test/Emulation and Enabling Real-Time Debugging Using FPGA for In-Circuit Emulation"; October 10, 2001; 09/975,104; Snyder
	T3	CYPR-CD00182; "In-System Chip Emulator Architecture"; October 10, 2001; 09/975,115; Snyder et al.
	U3	CYPR-CD00185; "Emulator Chip-Board Architecture and Interface"; October 1, 2001; 09/975,030; Snyder et al.
	V3	CYPR-CD00186; "Method for Breaking Execution of a Test Code in DUT and Emulator Chip Essentially Simultaneously and Handling Complex Breakpoint Events"; October 10, 2001; 09/975,338; Nemecek et al.
	W3	Anonymous; "Using Debug"; 1999; Prentice-Hall Publishing; pages 1-20

	X3	Harrison et al.; "Xilinx FPGA Design in a Group Environment Using VHDL and Synthesis Tools"; Colloquium on Digital System Design Using Synthesis Techniques; February 15, 1996; pages 5/1-5/4
	Y3	Microsoft Press Computer User's Dictionary; 1998; page 320
	Z3	Sreeram Duvvuru and Siamak Arya, "Evaluation of a Branch Target Address Cache", 1995, IEEE, pages 173-180
	A4	Andrew S. Tanenbaum with contributions from James R. Goodman, "Structured Computer Organization", 1999, Prentice Hall, Fourth Edition, pages 264-288, 359-362
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.  
Include copy of this form with next communication to applicant.